What is claimed is:

1. A semiconductor memory device comprising:

a first memory which is non-volatile; and

a second memory having a random access function, the first and second memories contained in one package, and the semiconductor memory capable of performing internal data transfer between the first and second memories,

wherein the second memory has an internal data transfer control signal that controls the internal data transfer, and an external transfer control signal that controls data transfer between an external CPU and the second memory,

the second memory incorporates a controller that controls data access to the first and second memories, and

when an access to the second memory is requested from the external CPU during the internal data transfer, the controller controls the internal transfer control signal so that the internal data transfer is suspend.

2. The semiconductor memory device according to claim 1, wherein the controller outputs a wait signal to request the external CPU to wait for access when the internal data transfer is suspended.

3. The semiconductor memory device according to claim 1, wherein the controller stores the address upon suspension when the internal data transfer is suspended, and restarts the transfer from the stored address when resuming the internal data transfer.

4. The semiconductor memory device according to claim 1, wherein the controller resumes the suspended internal data transfer when the external CPU does not access the second memory for a predetermined period during suspension of the internal data transfer.

5. The semiconductor memory device according to claim 1, wherein the controller has means for storing a bit that indicates a command for the suspension of the internal data transfer from the external CPU.

6. The semiconductor memory device according to claim 1, wherein the memory region of the second memory is divided into plural banks.

7. The semiconductor memory device according to claim 1, wherein the second memory is a memory having a dual port function.

8. The semiconductor memory device according to claim 1, wherein the controller transfers predetermined data stored in the first memory to a predetermined region in the second memory automatically when power of the semiconductor memory device is turned on.

9. The semiconductor memory device according to claim 8, wherein the controller stores transfer source address, transfer destination address and data amount of the transfer data, relating to the predetermined data.

10. The semiconductor memory device according to claim 8, wherein a memory region in the first memory is divided into plural sectors, and each sector has a flag showing whether the sector includes or not the data to be transferred automatically when the power is turned on.

11. The semiconductor memory device according to claim 8, wherein when the second memory requires a refreshing operation for stored data and the refreshing operation is applied only to specified regions, the region of the second memory for storing the data transferred automatically when the power turned on is set automatically to be the specified regions to which the refreshing operation is applied.